AMENDMENTS TO THE CLAIMS

1. (CURRENTLY AMENDED) ~~A circuit~~ An assembly comprising:

a database circuit configured to store a plurality pointer values for ~~each of~~ a plurality of first parameters ~~of~~ defined by a network protocol, wherein each one of said first parameters is associated with a corresponding one of said pointer values; and

a processing circuit configured to (i) process ~~at least~~ a particular one of said first parameters in an incoming packet received by said assembly in accordance with said corresponding pointer value to produce a second parameter and (ii) present an outgoing packet from said assembly containing said second parameter.

2. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 1, wherein (i) said database circuit is further configured to store ~~both an~~ a plurality of offset values and a plurality of length values for ~~each of the~~ said first parameters, each one of said first parameters is further associated with both a corresponding one of said offset values and a corresponding one of said length values and (ii) said processing circuit is further configured to partition said incoming packet in accordance with

~~both~~ at least one of said offset values ~~offsets~~ and at least one of said length values ~~lengths~~ to extract said particular first parameter ~~parameters~~.

3. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 2, further comprising an interface ~~directly connected to said database and configured to download all of said offsets, said lengths, and said pointers~~ through which said offset values, said length values and said pointer values are downloaded for storage in said database circuit.

4. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 1, wherein said processing circuit comprises:

a parsing circuit configured to partition said incoming packet;

a plurality of peripheral blocks ~~each~~ (i) coupled to said parsing circuit, (ii) identified by said pointer values ~~linked to said pointers~~ and (iii) configured to perform a plurality of processes ~~process~~ involving said first parameters; and

an assembling circuit coupled to said peripheral blocks and configured to generate said outgoing packet.

5. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 4, wherein said database circuit is further configured to

store both a second offset value and a second length value for said second parameter ~~of~~ as defined by a second network protocol.

6. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 4, further comprising an interface connectable to a peripheral block external to said assembly ~~circuit~~.

7. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 4, wherein said peripheral blocks are at least two circuits selected from a group of circuits consisting of a content addressable memory circuit, a time to live circuit, a comparison circuit, a counter circuit, a value swapping circuit, a stuffing circuit, a de-stuffing circuit, a cyclic redundancy checksum circuit, a parity circuit, a first-in-first-out circuit, a length construction generator circuit, a header error control synchronization circuit, a frame relay lookup circuit, a data link connection identifier circuit, a protocol identification analysis circuit, a point-to-point protocol verification circuit, a parameter discard circuit, and a buffer circuit.

8. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim ~~6~~ 4, wherein said peripheral blocks are configured to simultaneously processes a plurality of said first parameters.

9. (CURRENTLY AMENDED) The ~~circuit~~ assembly according to claim 1, wherein said processing circuit is implemented as only hardware.

10. (CURRENTLY AMENDED) An assembly comprising:

a first circuit configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet;

a second circuit configured to (i) store a plurality of pointer values for ~~each of~~ a plurality of first parameters ~~of~~ defined by said first network protocol, wherein each one of said first parameters is associated with a corresponding one of said pointer values, (ii) process ~~at least~~ a particular one of said first parameters in said incoming packet in accordance with said corresponding pointer value to produce a second parameter, and (iii) present an outgoing packet containing said second parameter; and

a third circuit configured to frame said outgoing packet to present a transmit frame to a second network.

11. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said second circuit is further configured to (i) store ~~both an~~ a plurality of offset values and a plurality of length values for ~~each of~~ said first parameters, each one of said first

parameters is further associated with both a corresponding one of said offset values and a corresponding one of said length values and (ii) partition said incoming packet in accordance with ~~both of~~ said offset values ~~offsets~~ and said length values ~~lengths~~ to extract said first parameters from said incoming packet.

12. (ORIGINAL) The assembly according to claim 10, wherein said first circuit is further configured to provided a plurality of frame delineation methods for a plurality of network protocols.

13. (ORIGINAL) The assembly according to claim 12, further comprising an interface configured to permit a selection among said frame delineation methods.

14. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said ~~second~~ third circuit is further configured to provided a plurality of framing methods for a plurality of network protocols.

15. (ORIGINAL) The assembly according to claim 14, further comprising an interface configured to permit a selection among said framing methods.

16. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said third circuit is further configured to delineate a second receive frame from said second network to produce ~~said~~ a second incoming packet.

17. (CURRENTLY AMENDED) The assembly according to claim 16, wherein said first circuit is further configured to frame ~~said~~ a second outgoing packet derived from said second incoming packet to present a second transmit frame to said first network.

18. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said first circuit comprises a plurality of framing circuits ~~each~~ configured to operate on a ~~unique network protocol~~ plurality of network protocols, wherein each one of said framing circuits operates on a corresponding one of said network protocols.

19. (CURRENTLY AMENDED) The assembly according to claim 10, wherein said third circuit comprises a plurality of de-framing circuits ~~each~~ configured to operate on ~~a unique network protocol~~ a plurality of network protocols, wherein each one of said de-framing circuits operates on a corresponding one of said network protocols.

20. (CURRENTLY AMENDED) The assembly according to claim 10, further comprising a fourth circuit connected to said second

circuit and configured process ~~at least~~ a select one of said first parameters in said incoming packet in accordance with said corresponding pointer value.